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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/981,603	10/17/2001	Robert F. Dvorak	NBD-48/47181-00259	7891

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EXAMINER	
BENENSON, BORIS	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 06/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/981,603	DVORAK ET AL.	
	Examiner	Art Unit	
	Boris Benenson	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-26,28-38,40 and 42-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *42,43 and 45-50* is/are allowed.

6)☒ Claim(s) *1-3,5-7,10,11,16-18,20,25,28-30,32,37 and 38* is/are rejected.

7)☐ Claim(s) *4,6,8-9,13-15,19,21-24,31,33-36,40, and 44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10/17/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/24-25/05, 4/8/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Actions

1. Information Disclosure Statements Received on 2/24/05, 2/25/2005, and 4/08/2005 have been considered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5-7, 10-11, 16-18, 20, 25, 28-30, 32, and 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blades (5,434,509) in view of Daum et al. (6,242,922).

Blades disclosed a Method And Apparatus For Detecting Arcing In Alternating-Current Power Systems By Monitoring High-Frequency Noise. Blades disclosed and claimed a method and an apparatus comprising steps and means for monitoring one of the line voltage and the load current and for extracting high-frequency noise therefrom, said high-

frequency noise being substantially higher in frequency than F; means for monitoring the extracted noise for detecting the occurrence of one or more bursts in the noise, said bursts having detectable properties characteristic of arcing, said detectable properties including one or more of rapid current rise time, frequency components in excess of 10 MHz, and broad frequency bandwidth; means for determining that arcing exists if said detected bursts, and/or a sequence of said bursts, satisfy one or more additional predetermined conditions; and means activated to produce an output signal responsive to the determination that arcing exists. Blades disclosed "When the derivative of the current has thus been determined, the microprocessor can compare the derivative of the current to a predetermined level and provide a signal that arcing may possibly be present when that derivative exceeds the predetermined level" Col.31, Lines 23-28). Blades doesn't disclose use of application specific integrated circuit (ASIC) into which all elements of the control circuitry are integrated. Daum et al. teach an Arc Detection Architecture Based On Correlation For Circuit Breakers. Daum et al. teach "Apparatus for detecting arcs from a signal provided by a current sensor includes a mixed analog digital

application specific integrated circuit (ASIC) employing a standard central processing unit (CPU) with a reduced digital signal processing (DSP) load and programmed to execute a correlation function for arc detection. Further, by enabling use of a standard CPU, fabrication cost of the ASIC can be substantially less than the fabrication cost associated with known arc detection units" (Col.1, Line 63 - Col.2, Line 6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified Blades with teachings of Daum et al. and integrate al circuits into an ASIC, because according to Daum et al. fabrication cost of the ASIC can be substantially less than the fabrication cost associated with known arc detection units.

Referring to Claims 2-3, 5, 17-18, 20, 29-30 and 32, Blades disclose use of "Score" counter. Beside Blades and Daum et al. disclose use of microprocessor that inherently uses number of hardware and software counters.

Referring to Claims 10-11, 25-26 and 37-38, Blades disclosed "a small LED is provided to indicate the presence of arcing before enough arcing has been detected to trip the breaker. It also serves to indicate, by

remaining illuminated, that the breaker tripped due to arcing and not overcurrent" (Col.7 Line 67-Col.8, Line 3). It is inherent that the interrupter latches and requires to be reset for further operations. The use of a buffer (capacitor) in order to accumulate energy and utilize stored energy is routine and should be claimed as an invention.

3. Claims 1-3,5,10,16-18,20,25, 28-30, 32, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Scott et al. (6,625,550) in view of Daum et al. (6,242,922).

Scott et al. disclose an Arc Fault Detection For Aircraft. Scott et al. disclose a "system for determining whether arcing is present in an aircraft electrical circuit comprising a sensor for sensing a current in said circuit and developing a corresponding sensor signal, a circuit for determining the presence in the sensor signal of broadband noise, and producing a corresponding output signal, and a controller for processing said sensor signal and said output signal in a predetermined fashion to determine whether an arcing fault is present in said circuit" (Col.6, Lines 23-32). Scott et al. disclose also that "there is

provided a controller for determining whether arcing is present in an aircraft electrical circuit in response to input signals, said input signals corresponding to a current in said circuit and to the presence of broadband noise in a predetermined range of frequencies in said circuit, said controller including a plurality of counters and wherein said controller increments said plurality of counters in a predetermined fashion in accordance with said input signals and periodically determines whether an arcing fault is present based at least in part on the state of said plurality of counters" (Col.6, Lines 34-43).

"The current samples are converted into current peak, current area, max (di/dt). These values are stored for each half cycle of voltage" (Col.9, Lines 19-21).

"The system analyzes these signals to determine whether an arcing fault is present, and if so, outputs a trip signal which may be used directly or indirectly to trip a circuit breaker or other circuit interruption device" (Abstract).

Scott et al. disclose "In one embodiment, the components of the arcing fault circuit detector 24 and the current measuring circuit 26 are provided on an application specific integrated circuit (ASIC) 30" (Col.8, Lines 13-16). Daum et al. teach "Apparatus for detecting arcs from a

signal provided by a current sensor includes a mixed analog digital application specific integrated circuit (ASIC) employing a standard central processing unit (CPU) with a reduced digital signal processing (DSP) load and programmed to execute a correlation function for arc detection. Further, by enabling use of a standard CPU, fabrication cost of the ASIC can be substantially less than the fabrication cost associated with known arc detection units" (Col.1, Line 63 - Col.2, Line 6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified system of Scott et al. and integrate all the element into ASIC as it is done in one of the embodiments, because it will decrease a manufacturing cost.

Referring to Claims 10-11, 25-26 and 37-38, the system generates "trip_signal". It is inherent that the interrupter latches and requires to be reset for further operations. The use of a buffer (capacitor) in order to accumulate energy and utilize stored energy is routine and should be claimed as an invention.

Allowable Subject Matter

4. Claims 42-43 and 45-50 are allowed.

5. Claims 47-50 are allowable because none of the prior art of record disclose an arc fault circuit interruption system that includes a test signal buffer which acts as a current source for driving a test winding at a center frequency of each of the bandpass filters in combination with the other claim limitations.
Claims 42-43 and 45-46 are dependent on allowable Claims 47, 48 and therefore allowable.

6. Claims 4, 6, 8-9, 13-15, 19, 21-24, 31, 33-36, 40 and 44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Boris Benenson whose telephone number is (571) 272-2048. The examiner can normally be reached on M-F (8:20-6:00) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2800 ext 36. The fax phone number

for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Boris Benenson
Examiner
Art Unit 2836

B.B.

Stephen W. Jackson
6-7-05

STEPHEN W. JACKSON
PRIMARY EX.